APPLICATION NOTE

DPC7146
NetLook Videoconferencing
Development Kit

AN98037

DPC7146 NetLook Videoconferencing Development Kit Version 1.0	Application Note AN98037

Abstract

The DPC7146 NetLook Videoconferencing Development Kit is a high performance solution for developing video conferencing systems for PCs with a PCI-bus architecture. It is based on Philips' proven desktop video architecture, allowing quick time-to-market and low risk development.

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SAA7146A Multimedia Scaler and PCI Bridge
NetLook Videoconferencing
SAA7111A Video Input Processor
SAA7185B Digital Video Encoder
TDA1309H
TDA1308
PCI bus mastering
Video and Audio Capture and Playback via PCI
VMI Video Modul Interface

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Summary

This document provides a description of the DPC7146 NetLook videoconferencing development kit. It gives detailed information about the development board and an outline of the software development kit. Due to the size of the SDK documentation, the detailed description of the SDK is provided as a seperate document. Further documentation about register setting of the INI-file and the debugger utilities are also dedicated and separated documents. This prevents, that the complete documentation has to be updated when an update of just one module is introduced. Documentation of the products published by companies other than Philips Semiconductors is also provided as seperate documents.

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1. Introduction

The DPC7146 NetLook development kit is a high performance solution for developing video conferencing systems for PCs with a PCI-bus architecture. It is based on Philips' proven desktop video architecture, allowing quick time-to-market and low risk development.

As well as the board itself, the ready-to-use NetLook kit includes Philips' control and video capture software and a camera. It also includes well-known videoconferencing packages. Standard device drivers for Microsoft Windows ensure the compatibility with all major video conferencing software. Together with the comprehensive set of software tools allowing rapid development of specific videoconferencing applications, designers can focus on product differentiation, a key success factor in this market.

This document provides a description of the NetLook videoconferencing development kit. It gives detailed information about the development board and an outline of the software development kit. Due to the size of the SDK documentation, the detailed description is provided as a seperate document. Further documentation about register setting of the INI file and the debugger utilities are also dedicated and separated documents. This prevents, that the complete documentation has to be updated when an update of just one module is introduced. Documentation of the products published by companies other than Philips Semiconductors is also provided as seperate documents.

1.1 Overview

The DPC7146 NetLook videoconferencing development board is intended to provide a platform for the development of videoconferencing systems. The compression algorithms can be performed in software or, after connecting a daughter board with an appropriate chip set, in hardware. The board has been designed in such a way, that the connection of daughter boards via standardised connectors is easily done.

The board is not limited to videoconferencing appliactions, but can also be used for every kind of video capture and playback and is therefore a powerful and versatile development tool.

The board features the following ICs:

SAA7146A   The SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* is a versatile PCI Bus interface chip allowing several video and audio data streams to be processed in parallel and transferred via PCI bus. The SAA7146A operates as bus master. It has 2 video input/output ports, 5 audio ports, 4 programmable I/O signals and one ISA bus-like interface (DEBI = Data Extension Bus Interface) for connection of MPEG decoders and other peripheral devices. The internal register programming sequencer allows autonomous execution of two tasks like individual scaling of even and odd fields. This local data stream processing off-loads the host CPU.

SAA7111A   The SAA7111A *Video Input Processor* (VIP) is a digital multi standard decoder with analog input processing and clock generation. It supports 2 CVBS inputs and one S-VIDEO input. The implemented A version operates under 3.3 V power supply.

SAA7185B   The SAA7185B *DENC* is a low cost digital video encoder providing several outputs.

TDA1309H   The TDA1309H combines low cost bit stream ADC and DAC for digital audio systems.

TDA1308   The TDA1308 is a low cost audio amplifier.

PCF8598E   The EEPROM PCF8598E contains the identification data of the board and its vendor. It will be read out at the boot sequence of the PC.

For low-cost videoconferencing applications, only a digital video decoder and the PCI bridge are required. This solution is implemented in the MPC7146 board offered by Philips Semiconductors, thus completing the range of videoconferencing applications from the high to the low end.

2. NetLook Videoconferencing Development Kit

2.1 Content of NetLook

DPC7146 evaluation board
Philips Low Level drivers for Windows 3.1, Windows 95, and Windows NT4.0
Philips control and debugger software
Source code for Philips video capture sample application
The board's Gerber file and schematics (Protel format)
Videoconferencing software by VDOnet and Boxtop
Camera

2.2 Documentation of NetLook on CD-ROM

Datasheets of:
    SAA7146A, SAA7111A, SAA7185B, TDA1309H, and TDA1308
SPCI SAA7146 software description
Release note for the Windows 3.1/95 drivers
Release note for the Windows NT drivers
Description of debugger utilities
Furthermore, electronic documentation of the videoconferencing software is provided on the CD-ROM.

2.3 Software package for NetLook

The CD-ROM contains the following sofware
SDK_31.zip: Software development kit for Windows 3.1
SDK_95.zip: Software development kit for Windows 95
SDK_NT.zip: Software development kit for Windows NT 4.0
gerber.zip: The boards Gerberfile
schematics.zip: The board's schematics
iVisit.exe: Installation file for iVisit (Windows 95 version)
VDO.exe Installation file for VDOprofessional (Windows 95 version)

2.4 System requirements* for NetLook

IBM PC or PC compatible 486 66MHz PCI system (Pentium 90 MHz recommended)
Direct Draw recommended
available PCI slot
PCI compliant VGA or Super VGA board, with accessible frame buffer (supporting one or more of the color space formats supported by the SAA7146A).
Sound card
CD-ROM drive
Microsoft Windows 95, Windows 3.1 or NT (attention: the videoconferencing SW are Windows 95 versions only)
* These requirements are for Philips' software; 3rd party videoconferencing software may have additional or higher requirements

3. Installation of NetLook

Installation of software and hardware is to be done sequentially. First, the SAA7146A drivers have to be installed according to the installation procedure described in the software manual. For register setting, please see the specific info document. After successfull installation of the Philips drivers, the videoconferencing software is installed according to the guidelines given in the respective manuals.

4. HW Architecture of the PCI Bridge SAA7146A

4.1 The PCI Bridge SAA7146A inside the PC
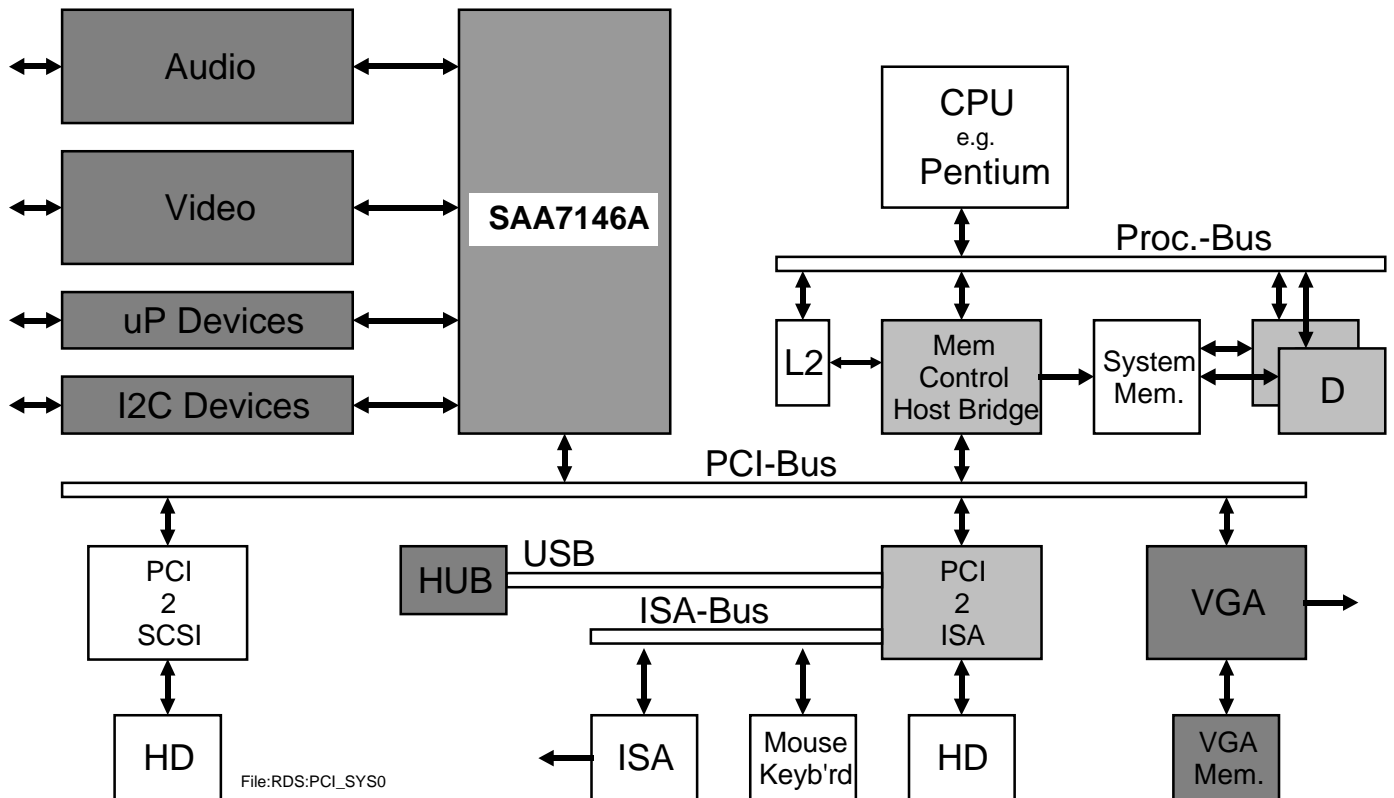
Fig.1 Architecture of a PC

A modern PC (= Personal Computer) consists of a CPU (CPU = Central Processing Unit), a PCI chip set, the memory, and a VGA. The HD (HD = Hard Disk), and the input devices of Keyboard and Mouse are completing a standard PC system. The PCI-chip set itself consists in general of the memory controller and PCI host bridge (Host Bridge), the system memory data buffers (D), and the PCI-to-ISA bridge.The system can be enhanced by units hooked to the PCI-bus or to the slower USB-Bus.

The PCI-bus is **the** high bandwidth bus inside the PC, with data rates of up to 132MByte/s (at 33MHz * 4 Byte). On this bus **all** information exchange is handled, except the traffic between the system memory (including the second level cache L2) and the CPU. The bus arbitration concept allows the access of every bus member in a certain order. This arbitration scheme is proprietary to the host bridge.

The CPU, e.g. a Pentium processor, does its data exchange via the processor bus to the second level cache L2 and/or the system memory. The memory management unit provides the access control for different memory types and its memory cycles. It also interfaces the CPU and the system memory to the PCI-bus with its different devices. The access structure to the PCI bus is adapted to the needs of the CPU in first instance.

The PCI-bus is operating in burst mode to achieve the maximum bandwidth performance. The maximum bandwidth of the PCI-bus is related to the clock speed of the CPU.

The host bridge arbitrates the bus and allows the access of every member to the bus in a certain order. Depending on the used PCI chip set this order might be different.

The PCI to ISA bridge is part of the PCI chip set. It interfaces not only to the ISA bus but also features connectivity to hard disk and CD player and other legacy devices like mouse and keyboard. All state-of-the-art PCI chip sets provide the USB bridge too, to allow easier Plug-and-Play interconnect concepts.

The VGA (VGA = Video Graphics Adapter) displays graphical objects and textual characters.

Aside the CPU as central processing unit, the SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* can take over the control of the PCI bus. Due to its local control possibilities it can control the data flows of audio, video, and other data streams through its interface.Therefor it off-loads the CPU. It can interface the system memory and/or the memory of the VGA with the audio, video, and other local systems.

4.2   The Architecture of the PCI Bridge SAA7146A

For multimedia over PCI, the SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* is the heart of the Philips' solution. It has many on-board interfaces, supporting video and audio inputs/outputs via the PCI interface, and has a high performance scaler core similar to that in the SAA7140. As a PCI bus master it can send data from its local sources of video, audio, and data interface (DEBI) to the main memory or it can request data from the memory. The data streams can be handled locally by powerful control engines. Operating autonomously, these engines (RPS and TSL) off-load the data control workload from the host CPU and enable real time control. The two RPS (RPS = register Programming Sequencer) engines can control in combination with the Local Event Management on almost all data streams, independent of the CPU. The TSL (TSL = Time Slot List) engines of the audio interface provide additional enhanced features to the SAA7146A like concurrent multi-channel input and output..
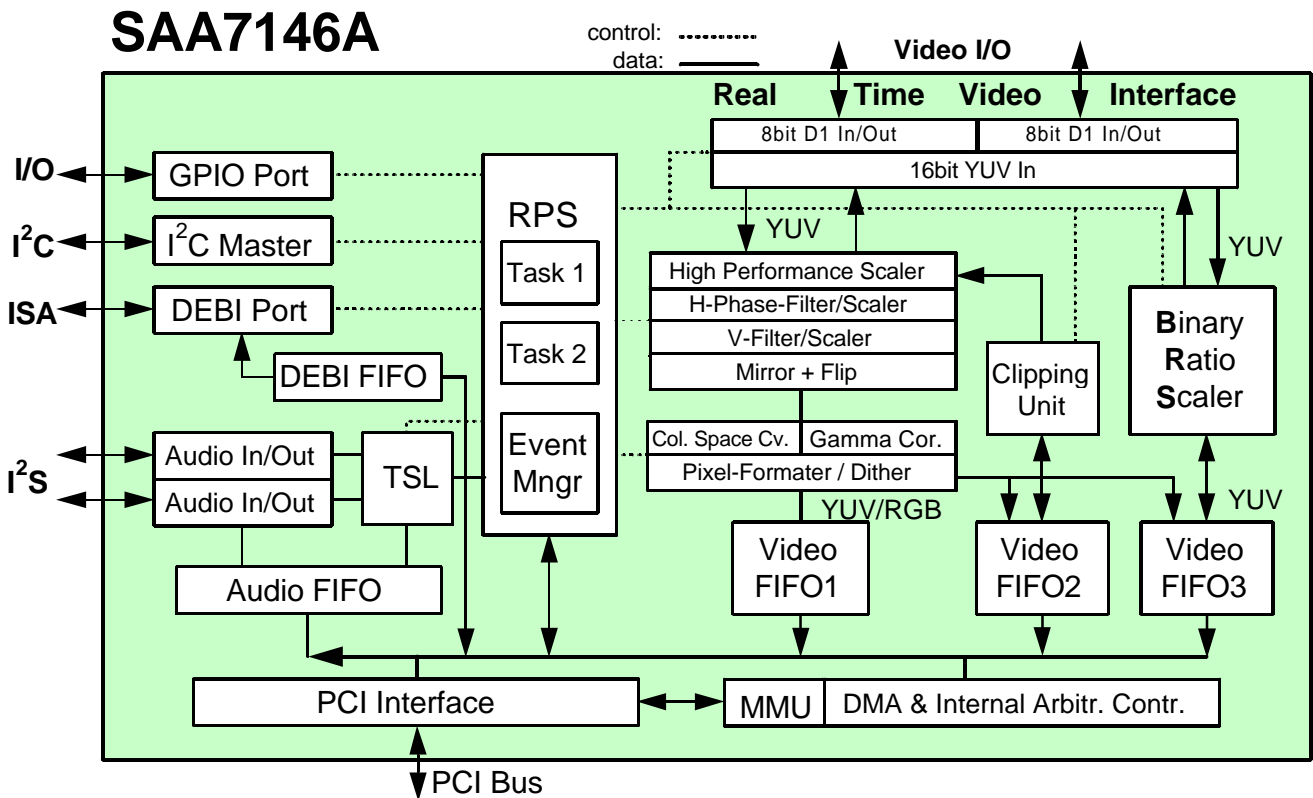
Fig.2 Architecture of the SAA7146A

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4.3   Blockdiagram

The DPC7146-V23 board deploys video and audio ICs and a range of interfaces and connectors. It is promoting the SAA7146A and provides with its connectivity a base for a range of functionality, where Videoconferencing is one solution aside to AC3-playback and MPEG-2 applications. But it also features the SAA711A, the TDA1309H, and the PCF8598E. The SAA7185B and the TDA1308 provide the output functionality of video and audio signals. The functions are placed on a 4-layered PCB of size 146 mm x 98mm (with out connectivity).
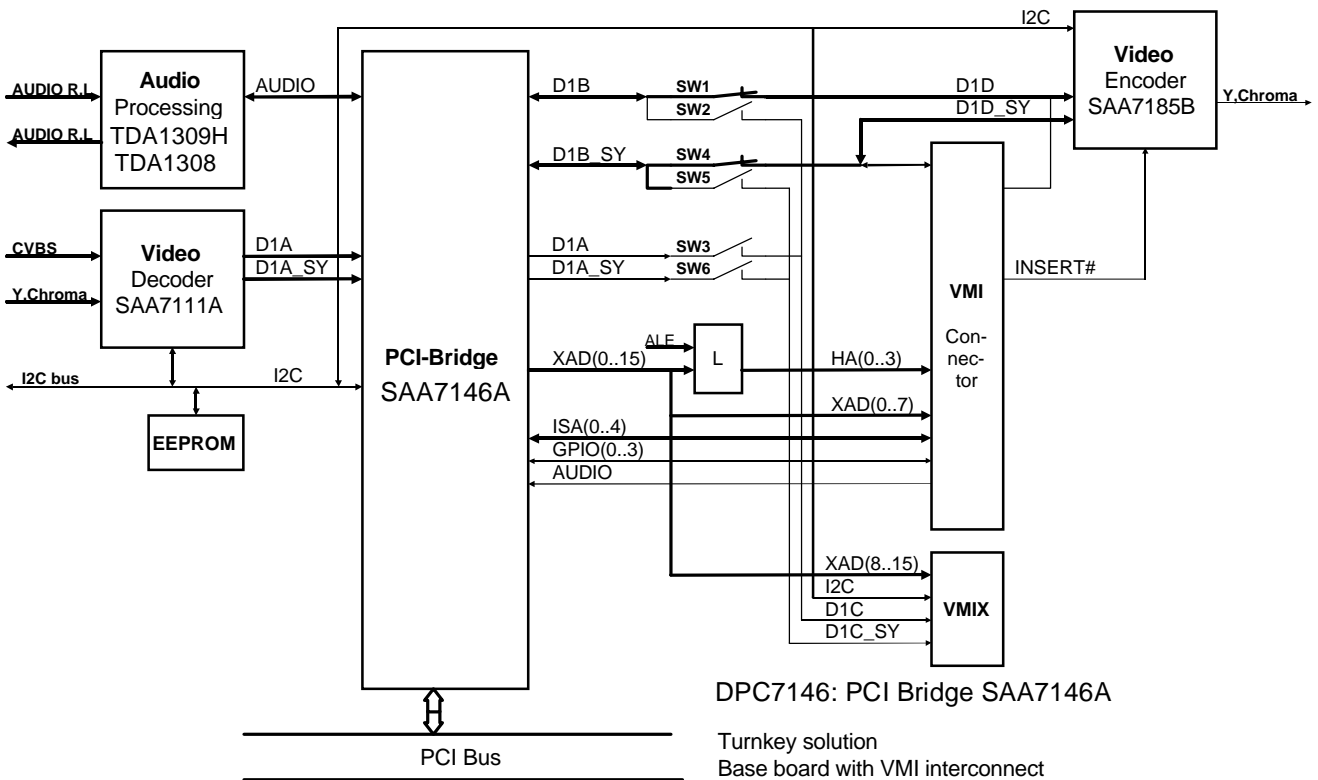
Fig.3 Blockdiagram of the DPC7146 V2.3 turn key board

The SAA7146A is the central component. It is controlled via the PCI bus. The data for identifying the board can be up-loaded from the EEPROM PCF8598E. This is a specific requirement from Windows95 specification (Windows95 is a trademark of Microsoft). With its two D1 ports it can provide simultaneous video-capture and video-play-back capability. The two independent audio I/O engines can be mapped on four of the 5 SD (SD = Serial Data) lines and on three of the 5 WS (WS = Word Select) lines arbitrarily. The DEBI port features either 8/16bit ISA bus style or the Motorola bus style. The GPIO interface and the multi-master I2C bus interface provide additional functionality.

5. Hardware Configuration

This chapter describes the hardware configuration of the DPC7146 V2.3 board.

- Board layout and placement of IC´s and connectors.

- PCI bridge: The SAA7146A interfacing and hardware configuration.

- Video Front End: The video decoders SAA7111 and SAA7111A.

- Daughter board connectivity with e.g. VMI connectivity.

- Video Back End: The video encoder block.

- Audio input and output: Audio clock generation, A/D and D/A conversion.

- Power supply.

The description of I/O signals can be found in the appendix.

5.1 Board Layout

All connectors and most of the ICs and other components are assembled on the top of the **4-layered** PCB board, as shown by the following figure. The parts on the soldering side are still inside the tolerated height, specified by the PCI SIG. The approach of 4 layers had been chosen to meet an optimum between cost and signal performance.

SAA7146:rds: b_layout.wmf
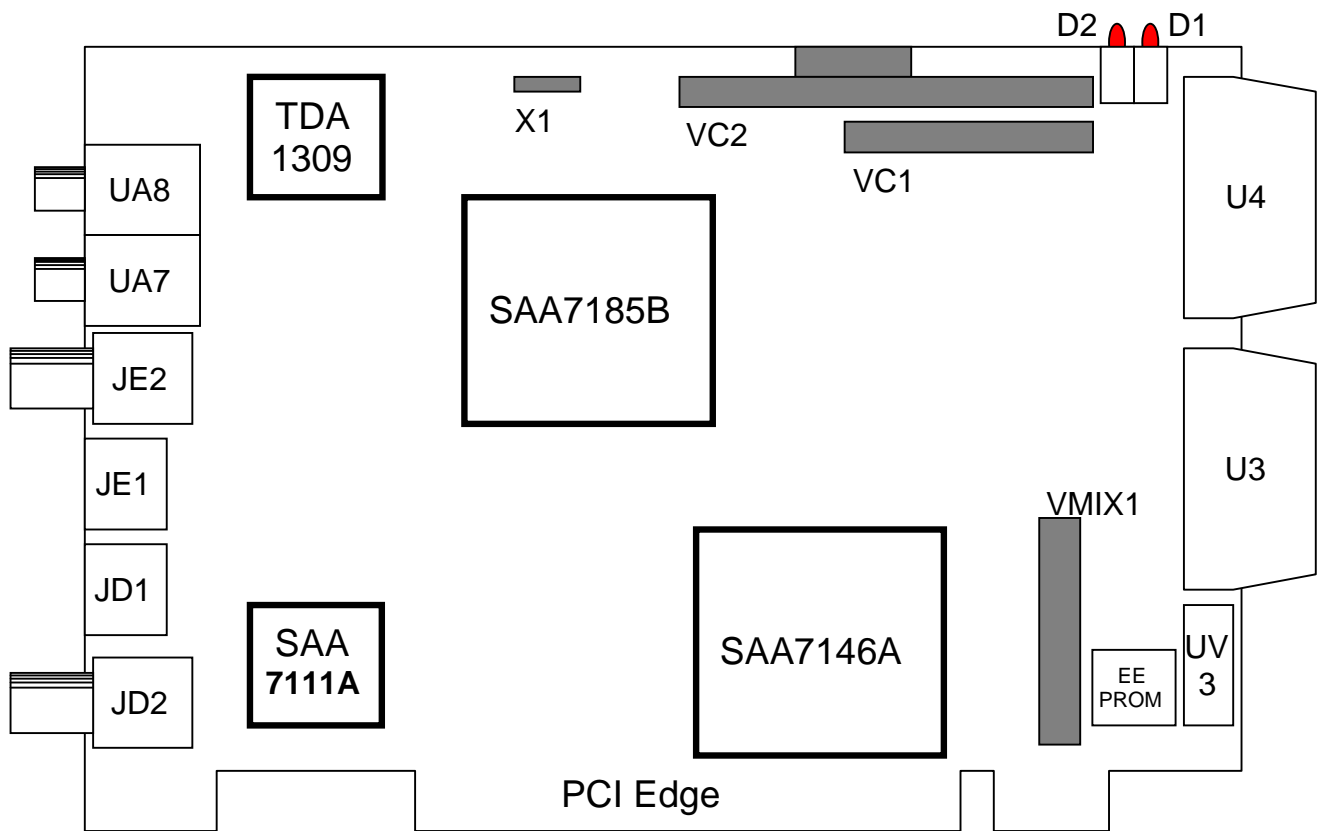
Fig.4 Board Layout of DPC7146-23

The following table lists all ICs used on the board:

TABLE 1 DPC7146: IC content

#	Device	Function
1	SAA7146A	PCI Bridge
2	SAA7111A	Video Decoder
3	SAA7185B	Video Encoder
4	PCF8598E	EEPROM
5	TDA1309H	Audio Codec
6	TDA1308	Head phone amplifier
7	74HC04	Inverter for audio clock generation
8	74HCT04	Inverter as LED driver
9	74F574	Latch for DEBI addresses
10	74F245	Driver for DENC signals to daughter boards

In the table below all connectivities are listed:

TABLE 2 DPC7146: Board Connector Overview

#	Connector	Function
1	PCI Edge	PCI Bus Edge Connector
2	JD1	S-Video Input + I2C Bus + 12V Power Supply
3	JD2	CVBS Video Input
4	JE1	S-Video Output
5	JE2	CVBS Video Output
6	UA7	Audio Input
7	UA8	Stereo Audio Output
8	U3	Digital Audio Connector
9	U4	Digital Audio Connector
10	UV3	I2C Bus Connector
11	VC1	Video Modul Interface Connector 1
12	VC2	Video Modul Interface Connector 2
13	VMIX1	Extended Video Modul Interface Connector
14	X1	Audio Clock Switch

The base line builds the PCI edge connector. Directly next it is the PCI bus master IC SAA7146A placed. Due to the short distance, the trace length of the PCI bus signals meet the PCI bus specification requirements. The limit is 1.5 inch for all PCI bus signals and 2.5 inch for the PCI CLK signal. The PCI CLK signal has a wounded track on the PCB to achieve this length. Only one clock load is allowed.
At the left side of the board, visible to the computer outlet, the analog video connectors are lined up. It starts with two video-in connectors (Cinch connector JD2 for CVBS and a S-Video connector JD1 with extra features). Two video-out follow (a S-Video connector JE1 and a Cinch connector JE2 for CVBS). The stereo audio-in connector UA7 and the audio-out connector UA8 complete the set.

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Opposite the PCI edge connector feature the two double LED (D1 and D2), which indicate the status of the GPIO pin's. Very close to them, the VMI connectors VC1 and VC2 provide the interface to e.g. a daughter board. Left to connector VC2, the audio clock switch X1 is placed.

At the right side, opposite to the analog connectors, the two digital audio connectors U3 and U4, and the I2C bus connector UV3 are placed. The digital audio data can be fed to an other board, e.g. a daughter board.

The video decoder SAA7111A block is grouped on a dense area close to the video-in connector. Due to the small board area and the short analog paths, this will not have any impact on the video performance.

The video encoder is placed more to the middle of the board area. This give room for the analog video post filter stages. The video signalling paths are shielded by a separate ground. This prevents distortion from other parts.

The audio codec TDA1309 is placed at the edge of the board, close to the connectors. This enables a good audio performance. The output amplifier TDA1308 is on the soldering side, to provide a dense packaging of the audio codec module.

The EEPROM is placed closed to the I2C bus connector. It contains the ID's of vendor and board. The complete content of the EEPROM is listed further below.

5.2   I2C Bus Port

The I2C bus is implemented as a bus master device.

At PC start up time a routine scans for a local EEPROM with subsystem, vendor ID support, maximum latency, and minimum grant. This is the expected case due to spec. The Philips part PCF8598E should be used.

5.2.1   Termination of I2C Bus

IMPORTANT: In case there is no local I2C bus device on the board, the I2C bus lines have to be pulled-up to VCC by resistors, to bring the port in a defined state! Otherwise the system might hang.

5.2.2   I2C Bus Connection between 5V and 3V Devices

The control of the video decoders is done by I2C bus signals. For connecting 3V devices with I2C bus devices operating on 5V rail, a circuitry of 3 components is proposed. Using a tuner with I2C bus interconnect, this can be handled by the S-Video connector JD1 which also supplies 12V power lines and the I2C bus signals to the external device.

Extra I2C bus connectivities are foreseen to control external devices. This I2C bus connectivity is normally not assembled. The connector can be placed in two ways to allow different connector arrangements.

The configuration settings for the SAA7111 and the SAA7111A which are explained below. The recommended decoder is the SAA7111A. This has been foreseen in the schematics.The I2C bus address can be selected by JV7.

The proposed I2C bus interface will transfer from 5 V of SAA7146A to 3 V environment.

5.3   Video Front End

The block consists of a multi standard video decoder of type SAA7111/11A with its passive components, a CVBS and a S-Video input connector and an I2C bus connector interface. The video decoder provides the colour decoded video data streams of one of the two video input sources.

The input is either an S-Video signal with separated luma and chroma components on connector JD1, or a CVBS signal on connector JD2. The unused analog inputs are grounded by a capacitor, to prevent distortion.

The decoded video is provided in 4:2:2 format as 8 bit wide data stream D1 format. The data are clocked by the LLC as V_SY3. The HREF or the HS can be assigned to the output signal V_SY1 by selector JP2. The V_SY0 contains the signal VS. The input signal FEIN is used, when video data buses are merged. The edges of LLC signal are damped by resistor RV20. It can be switched off by disassembling the resistor.

5.3.1   Video Clock

IMPORTANT: The video section with its DMA channels will not operate correctly, if no video clock is provided. The internal control is operating on this clock!

5.3.2   Decoder selection: SAA7111A versus SAA7111

Decoder SAA7111A:

The supply voltage is VCC_VIP = 3.3V.
The analog inputs ports of the SAA7111A expect a reduced video input swing. Therefore the termination resistors combination has to adapt the video input swing to the IC inputs. The values are as drawn:
   RV1 = RV3 = RV5 = 27R,
   RV2 = RV4 = RV6 = 47R

 Decoder SAA7111 (not implemented on the board):

The supply voltage is VCC_VIP = 5V.
The I2C bus input configuration of RV11, RV12, and UV2 is obsolete.
The video inputs are directly terminated by 75 Ohms:
   RV1 = RV3 = RV5 = 0R (Obsolete),
   RV2 = RV4 = RV6 = 75R

5.3.3   Layout considerations

The block of the video decoder should be placed on a separate ground plane. This concept is not completely realized, due to the required small placement area and the limited number of layers. The power supplies for the analog part and the digital one are separated and decoupled individually.
The +3.3V supply is generated from the +12V board supply. The decoupling capacitance should be realized by electrolytic and ceramic capacitors each with low inductance values. Instead of having a series inductance (LV2 of 2u2H) in the power rail, it is more recommended to use a simple series resistor of 4R7. For enhanced decoupling each pin might be decoupled individually by a RC-combination of 47nF and 10 Ohm. Small SMD packages like 0805 are recommended.

The supply for the analog part of the decoder can be treated in a similar way. The series inductance LV1 is replaced by a resistor of 4R7. A good ground plane layout and a shielding of the analog video signals is very much recommended. Due to the very dense layout this is not completely realized.

A short between the analog ground and the digital ground close to the decoder has been foreseen, but it is not used.

5.3.4   Switching the SAA7111A OFF

In some cases it is necessary to switch off the internal video decoder. to let another video source operate to the port A of the SAA71146A. For this case the actions are listed:

- Bring video data bus of SAA7111A into tri-state by pulling input pin FEIN from GND to VCC_VIP. This includes the removing of resistor RV8.
- Switch off the H and V sync signals and the CREF line by pulling input pin CE from VCC_VIP to GND. This includes the removing of resistor RV18.
- Remove resistor RV20 for disrupting the LLC clock line.
+ Introduce the new video signals, the new H and V sync signals, and the new clock signals of LLC and PXQ via VMI connector

For further details see section on "Non continuous video data streams to SAA7146A".

5.4   Video Back End

The block consists of the digital video encoder SAA7185B with its peripheral components, the output filter stages, and an S-Video output connector.

The digital video encoder operates in master mode. The clock and sync signals are generated and provided to the data source. The encoded analog video signals are fed via an output filter stage to the SVHS connector JE1 and the CVBS connector JE2.

The sync signals are buffered by a 74F245, to decoupled the encoder when the signals are used on the sub-board. The active high VIDSEL signal, used at direct play-back mode (DM), keys the video data to a standard colour value provided by a SAA7185B register.

5.5   Video Switch Matrix

The Video switch matrix interconnects the SAA7146A with the video front end SAA7111A, the video back end SAA7185B, and the VMI 1.4 connector plus extended connectors for connecting a daughter-board to the SAA7146A. The switches itself are laid out as set of resistors.

For standard use the switches SW1 and SW4 are closed and assembled with zero ohm resistors.The switches SW2, SW3, SW5, and SW6 are open assembled with resistors in order to minimize the components.

5.6   Audio Input/Output

The audio data output stage comprises of two parts: the audio input and output stage with a TDA1309 and the head-phone amplifier TDA1308T, and the audio clock oscillator.

5.6.1   Audio Performance

The analog audio performance has been measured inside an operating PC in a direct looping. It results in a total harmonic distortion of only 75dBTHD inside the audio band.

5.6.2   Audio Clock

The audio clock is generated by a crystal oscillator (here 11.2896 MHz, resulting in a sampling frequency of 44.1KHz).The output signal is distributed via two inverters on the board. The inverters are used to prevent line reflection from the oscillator. For using an external oscillator this clock can be switched off at connector X1. For default operation **pin3 and pin 4 have to be bridged!**

IMPORTANT: The audio engines of the SAA7146A will not operate correctly, if there no audio clock provided at the input. The internal control is operating on this clock! This holds also for situations when the audio section is in slave mode.

5.7   DEBI Port

The DEBI port features a ISA bus like interface when using the Intel mode. It can also be switched into the Motorola mode. The read/write signals as well as the address latching and ready signal are connected to the VMI-connector. When latching the addresses, devices of the FAST series (e.g. 74F574, 74F04) have to be used, to comply to the DEBI bus timing.

5.8   GPIO Port

The GPIO port consists of 4 lines which can be uses for standard level I/O signals as well as interrupt inputs. On the board they are connected to the VMI-connector VC2, and to a LED driver. A logical-High of the I/O pin switches the LED ON.

5.9   Daughter Board Connectivity

The board is equipped with a VMI 1.4 (Video Modul Interface) connector. It features one video output port with the appropriate synchronization signals. It is important to remark that the synchronization signals can operate in both directions. This gives the opportunity for digital encoders to operate in master mode. The VMI 1.4 specification mentions only a output direction of the synchronization signals.

The extended VMI connector enables the possibility for video I/O, which is not foreseen in the VMI spec. These video lines can be connected either to the A-port or to the B-port of the D1 interface.

The addresses for the data interface are latched by a register. An additional connector houses the further signals like the upper 8 bit of DEBI port Address/Data bus. This allows full 16 bit-transfer for the daughter board devices.

Two additional digital audio connectors interface external audio devices.

In standard operation mode the video data from SAA7146A will be fed to the digital encoder SAA7185B. This mode is also called Direct mode. Beside this mode other modes, like Line-Memory-Mode, and Field-Memory-Mode, are supported by the SAA7146A. These modes might be useful for special situations. They can be implemented via the provided connectivity.

5.10   Power Supply

Power supply of the board is splitted in different sections. The 12V supply of the PCI edge connector is used to generate the decoupled 3.3V supply and the analog 5V supply for the digital decoder, the digital encoder and the analog audio supply. The 5V supply of the PCI edge connector is used for a general supply of all standard 5V devices and it is used to generate the 3.3V supply of the SAA7146A. The reason for this splitting of the power supply is to decouple all parts from the main PC supply as well as from each other. This supports the concept of local decoupling of function blocks. The noise content of the video from a visual inspection is very little. The decoupling for the analog signals seems to be optimal even with respect to the large amount of digital components.

5.11   JTAG Pins

The SAA7146A follows the "IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture" set by the Joint Test Action Group (JTAG). Nevertheless a JTAG test procedure is not implemented on this board. Here some handling information:

- The TRSTN signal at pin 24 of SAA7146A should be connected to the PCI connector pin 1A, to comply to fully to the PCI specification.
- The pin TRSTN can, alternatively, be grounded to achieve the application mode.
- On the board the pin TRSTN is connected with the general PCI reset signal RSTN at pin 33 of SAA7146A. In this case the other test pins (TMS, TCLK, TDO, and TDI) should left open. The internal pull-up resistor prevent them from toggeling.

6. SW Structures

6.1 Architecture of 16 bit SW

The architecture of the 16 bit driver SW consists of the SAA7146.DLL and the SAA714x.VXD. The SAA7146.DLL has an object-oriented interface. The different high-level functional blocks like Video, DEBI, IIC, ArbCntrl, and EventCnt are operating in ring 3. Partly these blocks consist of several classes. They all access the HW of the SAA7146A via the IO class. The video classes are inherited from the scaler, and the clipper classes. The Event control resides in ring 3.

HW interrupts will be directly handled by the IO class.

The VXD SAA714x.386 is essentially responsible for the allocation of linear memory.

For details pls check the SAA7146 software description.
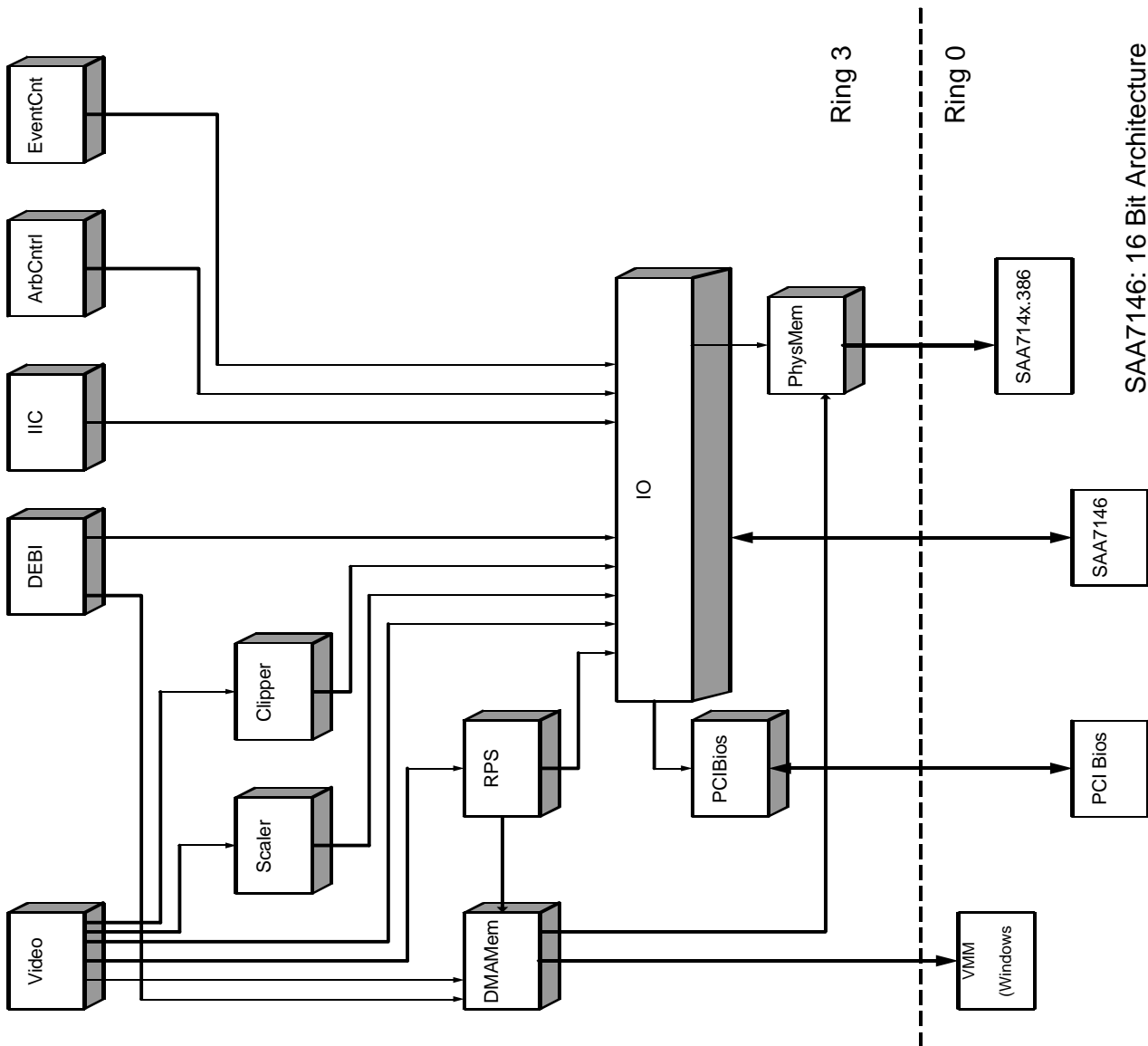
Fig.5 Architecture of 16 bit SW

6.2 Architecture of 32bit SW

The 32 bit architecture is different from the 16bit architecture in some parts. As in the previous version, one driver is operating in ring 3, while the other works from ring 0.

The access to the SAA7146A HW is done at ring 0 via the SAA7146.VXD. The HW interrupts are handled directly at the inner ring. An interface allows the access from other 3rd party VXDs.

The event control class is moved into the VXD with a remaining interface in ring 3. For faster access the DEBI class is also moved into ring 0, with similar constraints like the Event control class.
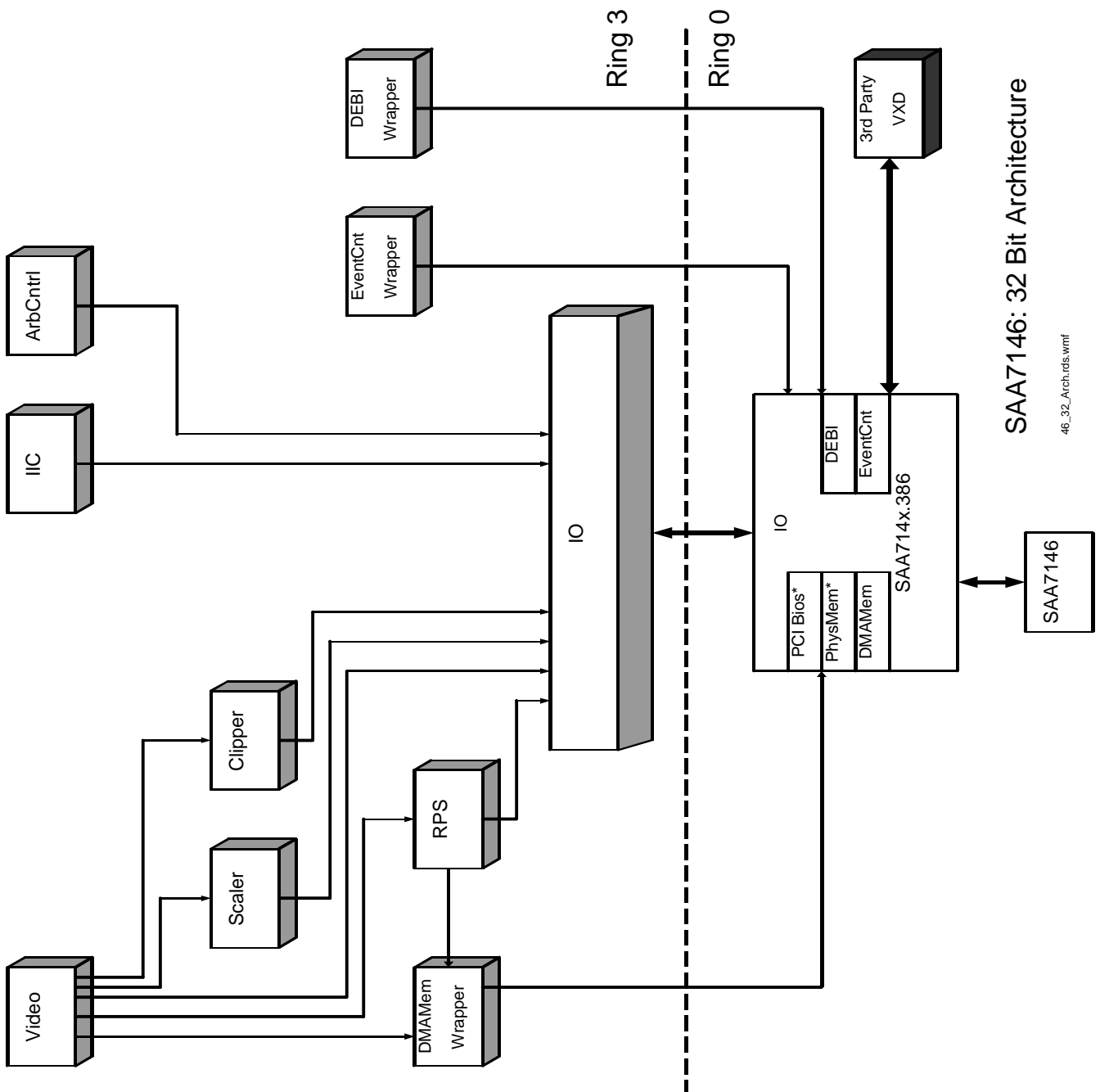
Fig.6 Architecture of 32bit SW

APPENDIX 1   PCI Commands of the SAA7146A

The PCI specification provides a set of commands to indicate to the target the type of transaction the master is requesting. The bus commands are encoded on the C/BE(3..0)# lines during the address phase. The SAA7146A utilises only a subset of these commands for its own purposes. These utilised commands differ between slave mode and master mode.

TABLE 3 PCI Commands used by SAA7146A

| C/BE(3..0)#	Command Type	Comments
0110	Memory Read	also used for Master Mode
0111	Memory Write	also used for Master Mode
1010	Configuration Read	
1011	Configuration Write	
1100	Memory Read Multiple	
1110	Memory Read	
1111	Memory Write and Invalidate	

APPENDIX 2   ID's at PCI Configuration Space of the SAA7146A

The PCI spec describes 4 different ID'sat the PCI configuration space.

TABLE 4 ID's at PCI Configuration Space

Address	NAME	BIT	TYPE		Description
00	Device ID	31-16	RO	7146H	SAA7146A
00	Vendor ID	15-0	RO	1131H	Philips
2C	Subsystem ID	31-16	RO	xxxxH	read from I2C EEPROM at PCI reset
2C	Subsys Vendor ID	15-0	RO	xxxxH	read from I2C EEPROM at PCI reset

The vendor ID 1131 is registered for Philips Semiconductors only. For further questions on PCI issues pls. contact the official entry point of the PCI Special Interest Group (SIG):

    PCI SIG
    2575 NE Kathryn #17
    Hillsboro, OR, 97124
    USA
    Ph   +1.503.693.6232
    fax   +1.503.693.8344
    email: pcisig@teleport.com or techsupp@pcisig.com

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APPENDIX 3   Organisation of EEPROM of the SAA7146A

The data of the subsystem ID and the subsystem vendor ID is organized in the EEPROM in the following order:

TABLE 5 Organisation of the EEPROM

Address in EEPROM	value	Place in Configuration Space
00	Subsystem ID (high byte)	byte: 2C, bits: 31 - 24
01	Subsystem ID (low byte)	byte: 2C, bits: 23 - 16
02	Subsys Vendor ID (high byte)	byte: 2C, bits: 15 - 8
03	Subsys Vendor ID (low byte)	byte: 2C, bits: 7 - 0
04	Max_Lat	byte: 3C, bits: 31 - 24
05	Min_Gnt	byte: 3C, bits: 23 - 16

APPENDIX 4   PCI Bus Connector of the DPC7146

The PCI connector interfaces the SAA7146A device with the PC system. All signals are standardised by PCI SIG.

TABLE 6 Board: PCI Bus Connector

Signal	I/O	Function
AD0..AD31	I/O	Address, Data lines for interconnect with PCI bus
C/BE0..C/BE3	I/O	Bus Command / Byte Enable
PAR	I/O	Parity Signal
PERR-	O	Parity Error
STOP-	I/O	Stop Signal
DEVSEL-	I/O	Device Select Signal
TRDY-	I/O	Target Ready Signal
IRDY-	I/O	Initiator Ready Signal
FRAME-	I/O	Frame Signal
IDSEL	I	Initialisation Device Select
GNT-	I	Bus grant input signal
REQ-	O	Bus request output signal
PCLK	I	PCI clock input signal
RST-	I	Device reset input signal
INTA-	O	Interrupt A

APPENDIX 5   Analog Video Inputs and Outputs of the DPC7146

The CVBS input connector and the S-Video input connector are feeding their video signals to the multi standards video decoder SAA7111/SAA7111A.

The S-Video input connector features additional to the video signals a power supply and an I2C bus connectivity to an external tuner or video camera device. Care should be taken, that the external device is capable of handling the **+12 V power supply**.
IMPORTANT: There is no fuse on the PCB for the supply voltage!.

TABLE 7 Board: Analog S-Video Input

Connector	Name	Pin	Signal
JD1	S-VIDEO1	1	GND
		2	GND
		3	Y (Luminance)
		4	C (Chrominance)
		5	SCL (I2C bus)
		6	**+12V**
		7	SDA (I2C bus)

TABLE 8 Board: Analog CVBS video Input

Connector	Name	Pin	Signal
JD2	CVBS	1	Composite Video
		2	GND

The CVBS output connector and the S-Video output connector are distributing their video signals from the multi standards video encoder SAA7185B. Holders of a macrovision licence, can use the SAA7184 alternatively.

TABLE 9 Board: Analog S-Video Output

Connector	Name	Pin	Signal
JE1		1	GND
		2	GND
	Y_OUT	3	Y (Luminance)
	C_OUT	4	C (Chrominance)

TABLE 10 Board: Analog CVBS video Output

Connector	Name	Pin	Signal
JE2	CVBS_OUT	1	Composite Video
		2	GND

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APPENDIX 6   Analog Audio Input and Output of the DPC7146

The stereo audio input is on connector UA7. The signals directly connect to the codec without any amplification.

TABLE 11 Board: Audio Input

Connector	Name	Pin	Signal
UA7	Audio Input	1	Left
		2	GND (analog)
		3	Right

The stereo audio output is on connector UA8. The codec signals are amplified by the head-phone amplifier TDA1308, which is on the soldering side of the PCB.

TABLE 12 Board: Audio Output

Connector	Name	Pin	Signal
UA8	Audio Output	1	Right
		2	GND (analog)
		3	Left

APPENDIX 7   Digital Audio Connectors

The digital audio connectors feature a bidirectional audio port to the SAA7146A. This feature has been used for an audio daughter board.

TABLE 13 Board: Digital Audio Connector

Connector	Name	Pin	Signal
U3	NC	1, 9	NC
	GND	2, 4, 6, 8, 10	GND
	A_BCLK0	3	Bit Clock
	A_WS3	5	Word Select
	A_SD3	7	Serial Data

TABLE 14 Board: Digital Audio Connector

Connector	Name	Pin	Signal
U4	NC	1, 9	NC
	GND	2, 4, 6, 8, 10	GND
	A_BCLK1	3	Bit Clock
	A_WS4	5	Word Select
	A_SD4	7	Serial Data

APPENDIX 8   I2C Bus Connector of the DPC7146

The I2C bus connector is placed on the board for auxiliary purpose. Other I2C bus devices inside the PC can be controlled, or the devices on the board can be controlled without the use of the SAA7146A. The connector is mounted in the new fashion of pinning. On behalf there might be older pinning version used, the connector can be slightly shifted to fit to another pinning. Please check the pinning of your I2C bus connector.

TABLE 15 Board: I2C Bus Connector

Connector	Name	Pin	Signal
UV3	SCL	1	Serial Clock
	GND	2	GND
	SDA	3	Serial Data
	VCC	4	5 V supply

TABLE 16 Board: I2C Bus Connector: Old Pinning when modified

Connector	Name	Pin	Signal
UV3: Old Pinning	VCC	1	5 V supply
	SDA	2	Serial Data
	GND	3	GND
	SCL	4	Serial Clock

APPENDIX 9   Schematics

The following pages contain the complete set of board schematics.

DPC71462.eps

VIP.eps

SPCI.eps

SAA7146.eps

DENC.eps

AUDIO.eps

POWER.eps